REMARKS

Applicants acknowledge receipt of the Examiner's Communication mailed August 7, 2000. The Communication refers to Applicants Preliminary Amendment filed July 24, 2000. Applicants filed the Preliminary Amendment to disclose a number of applications filed by the Applicants that may be considered to contain subject matter related to the subject matter of the present application. Applicants apparently inadvertently filed the Preliminary Amendment after the Examiner issued the June 26, 2000 Office Action. Accordingly, Applicants respectfully request the Examiner to enter the Preliminary Amendment, and consider the present Amendment as a formal response to the June 26, 2000 Office Action.

By this Amendment, Applicants have amended claims 1, 23, 30, 50 and 51, canceled claim 3, and added new claims 59-61. Therefore, claims 1, 2 and 4-61 are presently pending. Applicants respectfully request reconsideration, reexamination and allowance of the application.

The Examiner has rejected claims 1-5, 19, 23, 25-27, 29-31, 37, 44, 50, 51, 53-56 and 58 under 35 U.S.C. §102(e) as allegedly being unpatentable over Ben-Yoseph et al., U.S. Patent 5,949,439. The Examiner has also relied upon Ben Yoseph as a primary reference to support a rejection under 35 U.S.C. §103(a) that the remainder of the claims are allegedly unpatentable. Applicants have amended claim 1 to include the limitations of a graphics accelerator comprising a processor for processing graphics data; a data memory for storing the graphics data, the graphics data including pixels; a coprocessor for performing operations on a plurality of components of one pixel of the graphics data; and a direct memory access (DMA) engine for transferring the graphics data between external memory and the local memory. The Ben Yoseph et al. reference does not anticipate amended claim 1 because it fails to disclose the claimed combination including a DMA engine for

transferring the graphics data between external memory and local memory.

More particularly, Ben Yoseph discloses a multimedia processor 106 that uses Very Long Instruction Word (VLIW), vector processing, and single-instruction multiple data (SIMD) technology to achieve parallel operation. Col. 3, ll. 35-39. The processor includes a peripheral bus 125 with 14 virtual access channels for communicating with peripherals, such as audio stereo modem converter 118. Microprogrammable channels 0 to B are controlled by external devices and are used for DMA at a particular bandwidth. To enable the DMA operations, an external signal triggers a micro-program that transfers data to or from an external device. Col. 4, ll. 26-30; 34-40. Accordingly, Ben Yoseph merely discloses a peripheral processor that emulates a DMA for communicating with peripherals and for transferring a microprogram. There is no disclosure of using a DMA to transfer graphics data from memory. As Ben Yoseph fails to disclose an element of amended claim 1, Applicant respectfully requests allowance of claim 1 and claims dependent thereon.

As for method claim 30, Applicant has amended this claim to include the steps of loading a block of graphics data from main memory into local memory of a graphics accelerator having a processor and a coprocessor, the graphics data including pixels, each pixel having a plurality of components; performing operations on the plurality of components of each pixel of graphics data using the coprocessor; and concurrently transferring blocks of unprocessed data and processed data between the main memory and the local memory while the block of graphics data is being processed. There is no disclosure in Ben Yoseph of the claimed method including the concurrent transferring of graphics data between local memory and main memory as a block of data is being processed. Accordingly, Applicants respectfully request allowance of claim 30 and all claims dependent thereon.

Furthermore, Gulick, U.S. Patent 5,758,177, and Hancock, U.S. Patent 5,604,514, either alone or in combination with Ben Yoseph, fail to disclose the limitations of the claims rejected under 35 U.S.C. §103(a), or new claims 59-61. There is no disclosure or suggestion in the cited references for example, of processing graphics data while concurrently transferring processed and unprocessed blocks of graphics data between local memory and main memory. As the combination of references, either alone or in combination, fail to disclose or suggest the claimed inventions, they cannot support a rejection under 35 U.S.C. §103(a).

Based on the foregoing, Applicants submit that claims 1, 2 and 4-61 are in condition for allowance. Applicants therefore respectfully request early issuance of a Notice of Allowance.

Respectfully submitted,

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